THAPAR POLYTECHNIC COLLEGE PATIALA

BRANCH ELECTRICAL/ 4th SEMESTER

Subject: Digital Electronics

ASSIGNMENTS

Assignment-2

1. a) How AND gate can be obtained from NAND gate.

   B) How NOT gate can be obtained from NOR gate.

2. Define the following terms regarding a logic family:

   a) Noise margin b) Propagation delay

3. Evaluate $xy + \overline{xz} + x\bar{y}z(xy + z)$

4. Draw a karnaugh Map to reduce the function. Realize the reduced function by using NAND Gates.

$$F = \sum m(0,1,4,5,12,13,8,9,2,6,14)$$

5. Simplify the SOP expression.

$$f(A,B,C,D) = \sum m(1,3,7,11,15) + d(0,2,5)$$

Where *d* denotes don't care condition.

6. Explain the laws related to boolean algebra.

7. Write short note on 4 bit adder circuit.

8. Diff. B/w combinational circuit and Sequential circuit.

9. Write short note on Light Emitting Diode and LCD.

Assignment-3

1.Design a 1:4 and 1:8 DEMUX.

2.Explain the working principle of JK Master/Slave flip flop and draw its truth table.

3.Give application of flip flops.

4.What do you mean by ripple counter.

5.Diff. B/w synchronous and asynchronous counters.

6.Explain working and construction of a successive approximation type of ADC.

SEMINAR TOPICS

Sr. no.	Seminar Topics	Roll no.
1	Types of Flip Flops, Master Slave Flipflop, Applications of Flip Flop	81-92
2	Difference between Synchronous Counter and Asynchronous Counters, Modulus Counter, Ring Counters	93-109
3	Types of Shift Registers, universal Shift Register, Applications of Shift register	101-118
4	Types of Analog to Digital Converters, Multiplexer and Demultiplexer	119-134
5	Types of Digital to analog converters, Encoder and Decoders	136-150
6	Explain Full adder circuit with the help of truth table, Light emitting diodes, LCD	151-180

Youtube links

https://www.youtube.com/watch?v=-paFaxtTCkI&list=PLuYnCh-Sh1XeMNOdfvgPmnTPelkscZdxP

https://www.youtube.com/watch?v=yOW-JsJL1Ks&list=PLuYnCh-Sh1XeMNOdfvgPmnTPelkscZdxP&index=7

https://www.youtube.com/watch?v=yqg1sqhZG3M

https://www.youtube.com/watch?v=AEGzpMlOsvc&list=PLuYnCh-Sh1XeMNOdfvgPmnTPelkscZdxP&index=6

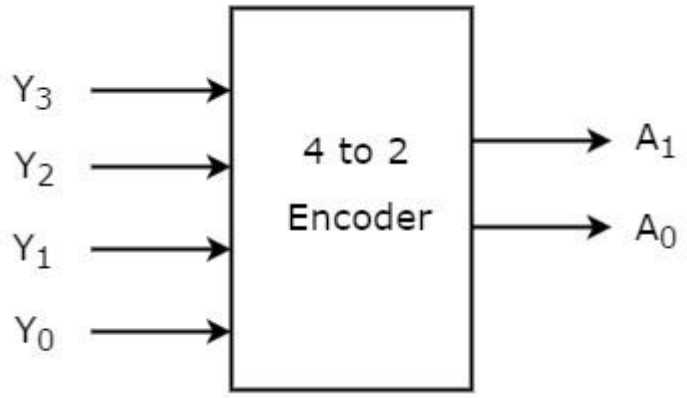
https://www.youtube.com/watch?v=HicZcgdGxZY&list=PLwjK_iyK4LLCnW-df-_53d-6yYrGb9zZc

Notes

An **Encoder** is a combinational circuit that performs the reverse operation of Decoder. It has maximum of 2^n input lines and 'n' output lines. It will produce a binary code equivalent to the input, which is active High. Therefore, the encoder encodes 2^n input lines with 'n' bits. It is optional to represent the enable signal in encoders.

4 to 2 Encoder

Let 4 to 2 Encoder has four inputs Y_3, Y_2, Y_1 & Y_0 and two outputs A_1 & A_0. The **block diagram** of 4 to 2 Encoder is shown in the following figure.



At any time, only one of these 4 inputs can be '1' in order to get the respective binary code at the output. The **Truth table** of 4 to 2 encoder is shown below.

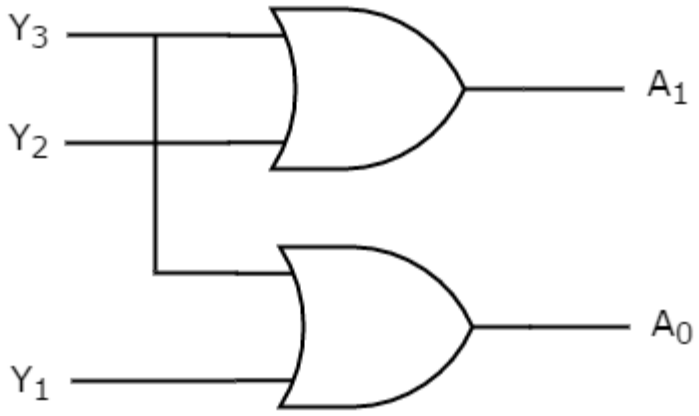
Inputs				**Outputs**	
Y_3	**Y_2**	**Y_1**	**Y_0**	**A_1**	**A_0**
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

From Truth table, we can write the **Boolean functions** for each output as

$$A_1=Y_3+Y_2 A1=Y3+Y2$$

$$A_0=Y_3+Y_1 A0=Y3+Y1$$

We can implement the above two Boolean functions by using two input OR gates. The **circuit diagram** of 4 to 2 encoder is shown in the following figure.



The above circuit diagram contains two OR gates. These OR gates encode the four inputs with two bits

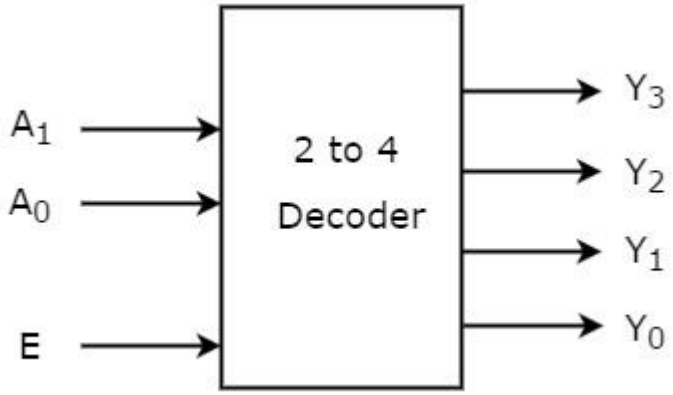
Multiplexer is a combinational circuit that has maximum of 2^n data inputs, 'n' selection lines and single output line. One of these data inputs will be connected to the output based on the values of selection lines.

Since there are 'n' selection lines, there will be 2^n possible combinations of zeros and ones. So, each combination will select only one data input. Multiplexer is also called as **Mux**.

Decoder is a combinational circuit that has 'n' input lines and maximum of 2^n output lines. One of these outputs will be active High based on the combination of inputs present, when the decoder is enabled. That means decoder detects a particular code. The outputs of the decoder are nothing but the **min terms** of 'n' input variables lineslines, when it is enabled.

2 to 4 Decoder

Let 2 to 4 Decoder has two inputs A_1 & A_0 and four outputs Y_3, Y_2, Y_1 & Y_0. The **block diagram** of 2 to 4 decoder is shown in the following figure.



One of these four outputs will be '1' for each combination of inputs when enable, E is '1'. The **Truth table** of 2 to 4 decoder is shown below.

Enable	Inputs		Outputs			
E	**A_1**	**A_0**	**Y_3**	**Y_2**	**Y_1**	**Y_0**
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

From Truth table, we can write the **Boolean functions** for each output as

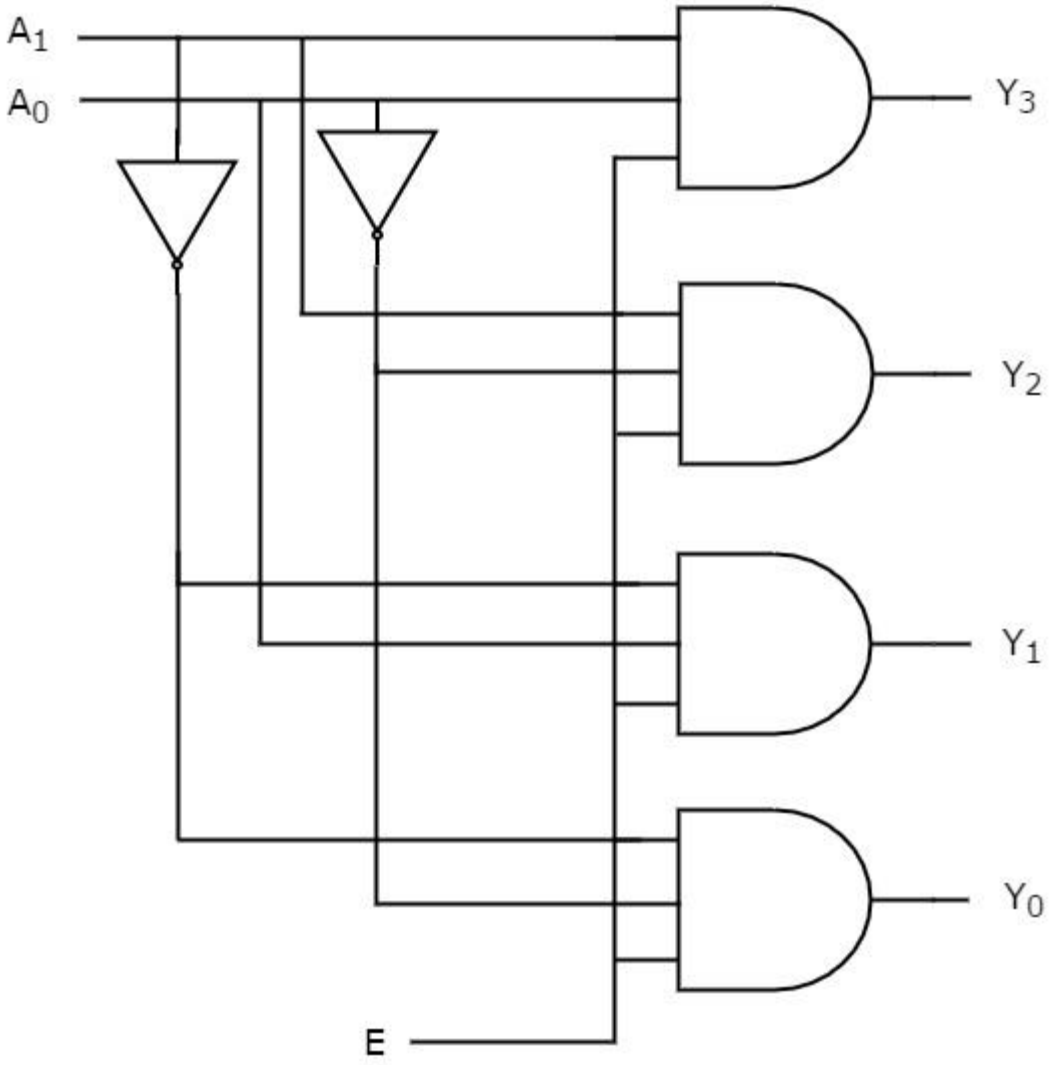
$$Y3=E.A1.A0Y3=E.A1.A0$$

$$Y2=E.A1.A0′Y2=E.A1.A0′$$

$$Y1=E.A1′.A0Y1=E.A1′.A0$$

$$Y0=E.A1′.A0′Y0=E.A1′.A0′$$

Each output is having one product term. So, there are four product terms in total. We can implement these four product terms by using four AND gates having three inputs each & two inverters. The **circuit diagram** of 2 to 4 decoder is shown in the following figure.

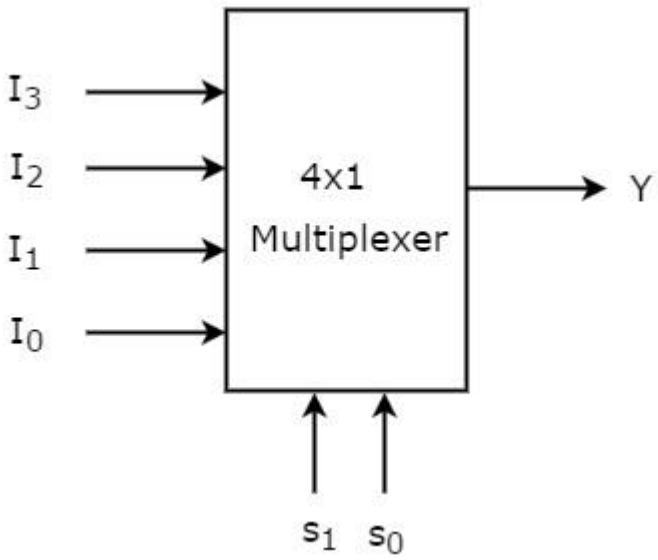


Therefore, the outputs of 2 to 4 decoder are nothing but the **min terms** of two input variables A_1 & A_0, when enable, E is equal to one. If enable, E is zero, then all the outputs of decoder will be equal to zero.

Similarly, 3 to 8 decoder produces eight min terms of three input variables A_2, A_1 & A_0 and 4 to 16 decoder produces sixteen min terms of four input variables A_3, A_2, A_1 & A_0.

4x1 Multiplexer

4x1 Multiplexer has four data inputs I_3, I_2, I_1 & I_0, two selection lines s_1 & s_0 and one output Y. The **block diagram** of 4x1 Multiplexer is shown in the following figure.

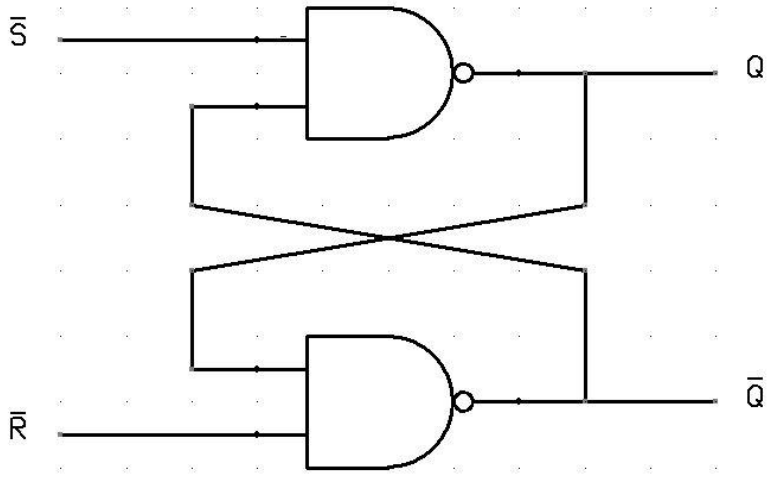


Flip flop v/s Latch

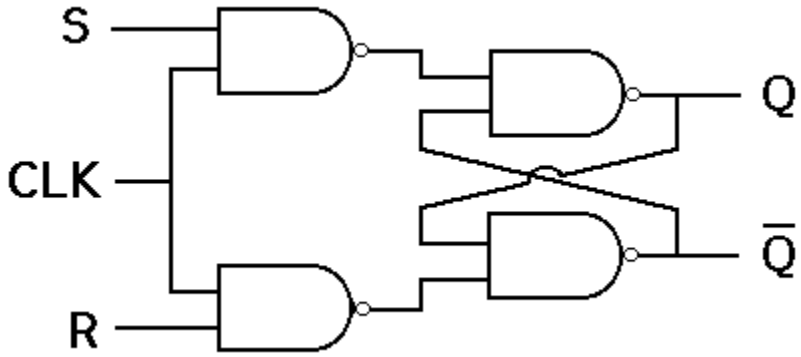
The basic difference between a latch and a flip-flop is a gating or clocking mechanism.

Read the full comparison of Flip Flop v/s latcH

For example, let us talk about SR latch and SR flip-flops. In this circuit when you Set S as active the output Q would be high and Q' will be low. This is irrespective of anything else. (This is an active-low circuit so active here means low, but for an active high circuit active would mean high)



flip flop, on the other hand, is synchronous and is also known as gated or clocked SR latch.

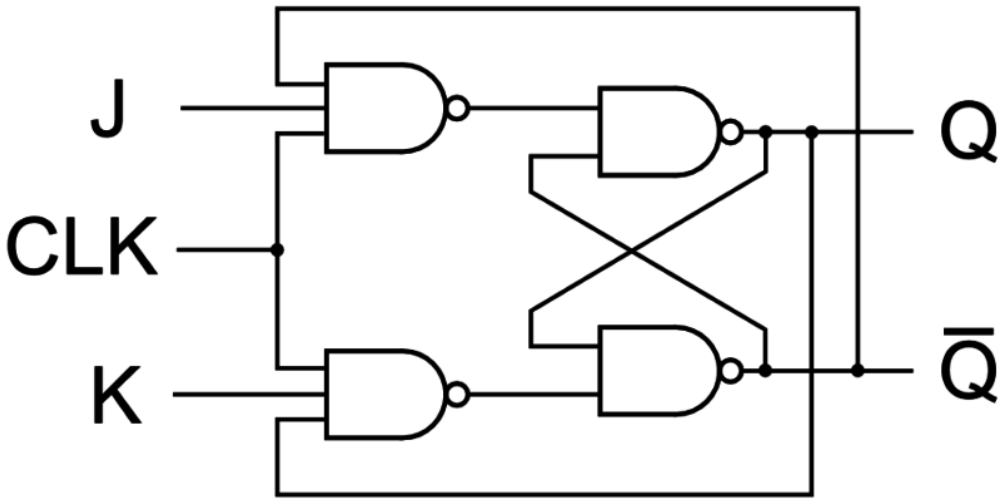


SR Flip-Flop

In this circuit diagram, the output is changed (i.e. the stored data is changed) only when you give an active clock signal. Otherwise, even if the S or R is active the data will not change.

JK Flip-flop

Due to the undefined state in the SR flip flop, another flip flop is required in electronics. The JK flip flop is an improvement on the SR flip flop where S=R=1 is not a problem.

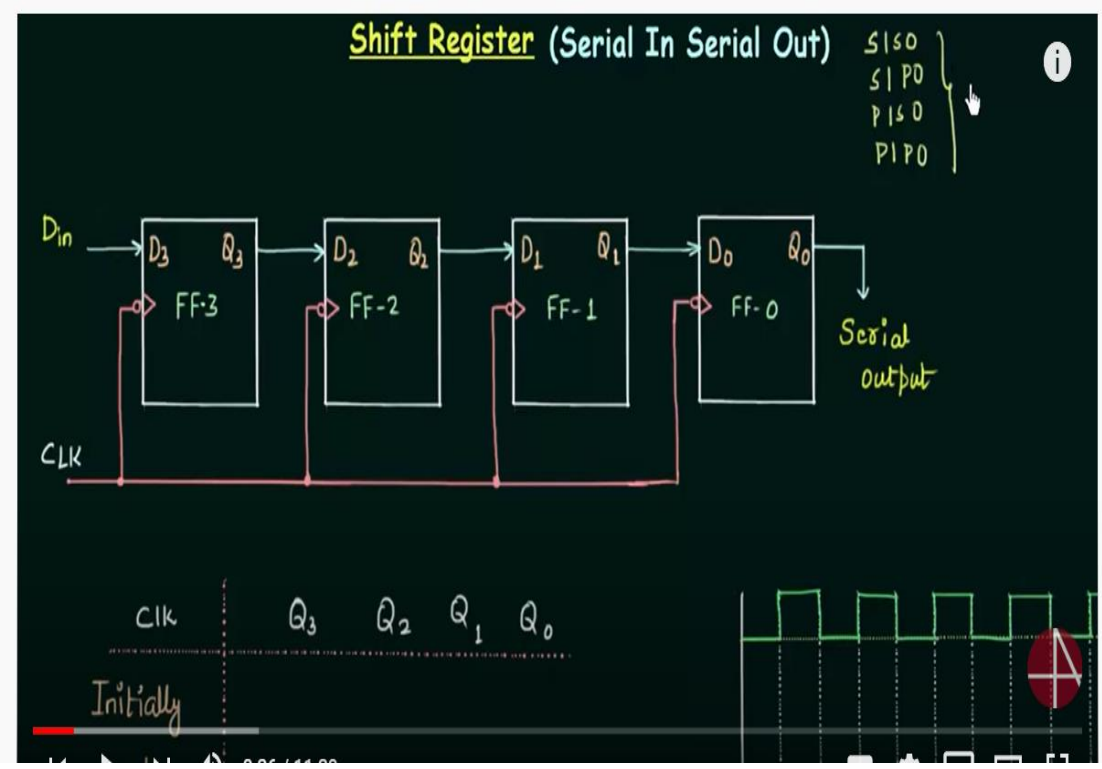


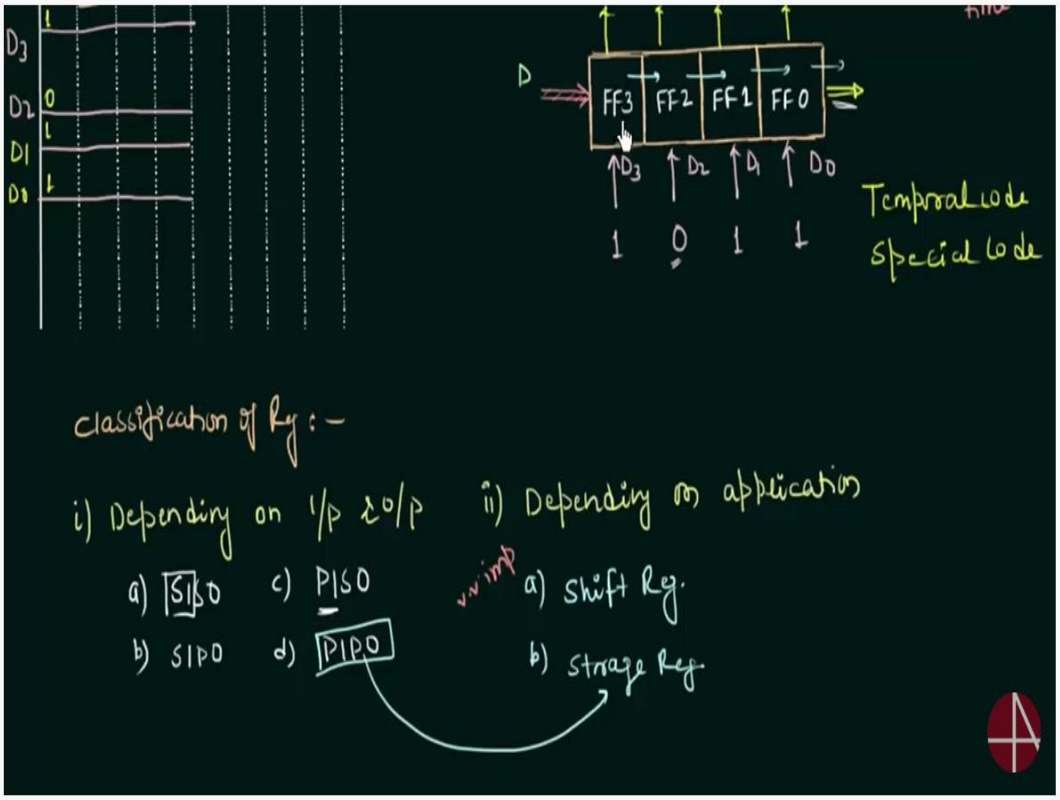
JK Flip-Flop

The input condition of J=K=1, gives an output inverting the output state. However, the outputs are the same when one tests the circuit practically.

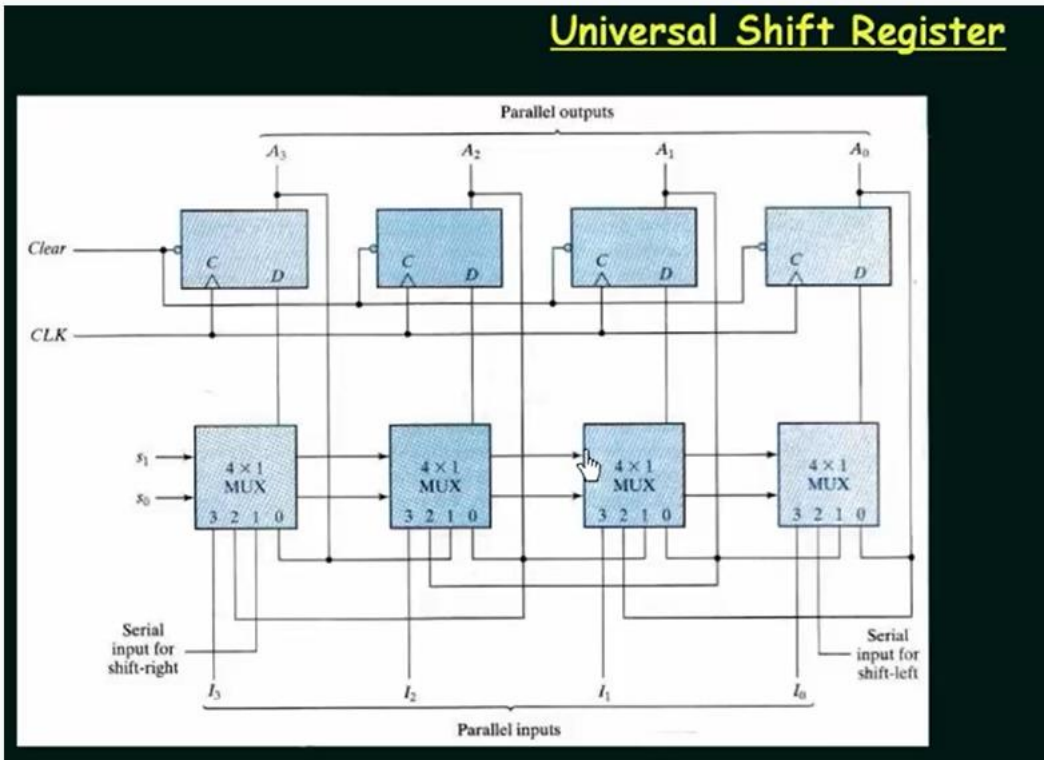
In simple words, If J and K data input are different (i.e. high and low) then the output Q

takes the value of J at the next clock edge. If J and K are both low then no change occurs. If J and K are both high at the clock edge then the output will toggle from one state to the other. JK Flip Flop can function as Set or Reset Flip flop





Data Formats and Classification of Registers



Asynchronous/Ripple Counter	Synchronous Counter
1. Flip flops are connected in such a waythat the o/p of first flip flop drives the clock of next flip flop.	1. There is no connection between o/p of first flip flop and clock of next flip flop.
2. Flip flops are not clocked simultaneously.	2. Flip flops are clocked simultaneously.
3. Circuit is simple for more number of states.	3. Circuit becomes complicated as number of states increases.
4. Speed is slow as clock is propagated through number of stages	4. Speed is high as clock is given at a same time.

Ring Counter

* no of states = no. of ff used

$= 2^4 : 16$

>> Ring counter is a typical application of shift register

>> The only change is the otput of last ff is connected to the input of first ff.